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Attorney Docket: 8021-174 (SS-18151-US)

Susan A. Guarascio
Susan A. Guarascio



Patent

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

Applicant: LEE, Jung-Bae Examiner: CHO, James Hyonchol
Serial No.: 10/716,120 Art Unit: 2819
Filed: November 18, 2003 Docket: 8021-174 (SS-18151-US)
Title: ON-DIE TERMINATION CIRCUIT AND METHOD FOR REDUCING ON-
CHIP DC CURRENT, AND MEMORY SYSTEM INCLUDING MEMORY
DEVICE HAVING THE SAME

Mail Stop Amendment
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

AMENDMENT

This paper is responsive to the Office Action mailed on June 8, 2005. The
Examiner is requested to enter and consider the following amendments and remarks.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

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By: *David J. Guasid*